IN THE CLAIMS

1. (Currently amended) A processor comprising:

at least a portion of a first split transmit and receive media access controller;

the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another;

wherein the processor comprises an interface for directing signals between the transmit unit and the receive unit of the first split transmit and receive media access controller, the interface being configured to multiplex the signals with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller;

wherein the first and second split transmit and receive media access controllers have respective distinct addresses encoded by particular values of information bits sent over the interface and the processor decodes said information bits so as to distinguish a first signal sent between the transmit and receive units of the first split transmit and receive media access controller from a second signal sent between the transmit and receive units of the second split transmit and receive media access controller.

2. (Original) The processor of claim 1 wherein one or more of the transmit units are implemented in a first region of an integrated circuit, and one or more of the receive units are implemented in a second region of the integrated circuit, remote from the first region.

3. (Original) The processor of claim 1 wherein one or more of the transmit units are implemented on a first integrated circuit and one or more of the receive units are implemented on a second integrated circuit.

4. (Original) The processor of claim 1 wherein the interface is controllably operable in one of at least two modes including an internal mode of operation, in which the interface is configured to deliver signals between one or more transmit units and one or more receive units where the transmit units and the receive units are implemented on the same integrated circuit, and an external mode of operation, in which the interface is configured to deliver signals between one or more transmit units

and one or more receive units where the transmit units and the receive units are implemented on different integrated circuits.

5. (Original) The processor of claim 1 wherein the interface comprises a receive interface block coupled to a generate interface block via an interface bus, the generate interface block receiving signals from a plurality of media access controller receive units and multiplexing the signals onto the interface bus for delivery to the receive interface block, the receive interface block demultiplexing the signals from the interface bus for delivery to appropriates ones of a plurality of media access controller transmit units.

6. (Original) The processor of claim 5 wherein the generate interface block multiplexes the signals onto the interface bus utilizing a plurality of round-robin arbiters.

7. (Original) The processor of claim 5 wherein the interface bus comprises a five-bit wide information signal bus and at least one clock signal line.

8. (Original) The processor of claim 5 wherein the interface bus comprises a separate dedicated information signal bus for delivering carrier sense signals between one or more of the receive units and one or more of the transmit units in an internal mode of operation of the interface.

9. (Original) The processor of claim 5 wherein the signals received by the generate interface block for delivery to the receive interface block comprise one or more of carrier sense signals, auto-negotiation signals, flow control signals, and deference reset signals.

10. (Original) The processor of claim 5 wherein the signals received by the generate interface block are multiplexed onto the interface bus using a priority-based selection mechanism which assigns the highest priority to the carrier sense signals, the second highest priority to the auto-negotiation signals, and lower priorities to the flow control and deference reset signals.

11. (Original) The processor of claim 5 wherein the receive interface block and the generate interface block operate in accordance with a state machine having at least a synchronization state, a control address state and one or more data states.

12. (Original) The processor of claim 11 wherein the control address state carries information regarding signal type and signal interface address.

13. (Original) The processor of claim 1 wherein the interface comprises a plurality of channels, each having one or more ports associated therewith, and wherein a given signal to be directed between transmit and receive units of a given split transmit and receive media access controller is assigned to a particular channel and port of the interface.

14. (Original) The processor of claim 13 wherein each of the channels may have up to eight ports, with a single-bit nibble address being utilized to identify a particular one of first and second four-port groups of a given eight-port channel.

15. (Original) The processor of claim 1 wherein the processor comprises an integrated circuit.

16. (Original) The processor of claim 1 wherein the processor comprises a network processor.

17. (Original) A method for use in a processor comprising at least a portion of a first split transmit and receive media access controller, the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another, the method comprising the step of:

multiplexing onto a common interface (i) signals to be directed between the transmit unit and the receive unit of the first split transmit and receive media access controller, and (ii)

signals to be directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller;

wherein the multiplexing step further comprises the step of:

associating the first and second split transmit and receive media access controllers with respective distinct addresses encoded by particular values of information bits sent over the interface;

wherein said information bits are decoded so as to distinguish a first signal sent between the transmit and receive units of the first split transmit and receive media access controller from a second signal sent between the transmit and receive units of the second split transmit and receive media access controller.

18. (Currently amended) A processor-readable storage medium for use in conjunction with a processor, the processor comprising at least a portion of a first split transmit and receive media access controller, the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another, the medium having embodied therein processor-executable instructions, the instructions when executed implementing the step of:

multiplexing onto a common interface (i) signals to be directed between the transmit unit and the receive unit of the first split transmit and receive media access controller, and (ii) signals to be directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller;

wherein the multiplexing step further comprises the step of:

associating the first and second split transmit and receive media access controllers with respective distinct addresses encoded by particular values of information bits sent over the interface;

wherein said information bits are decoded so as to distinguish a first signal sent between the transmit and receive units of the first split transmit and receive media access controller from a second signal sent between the transmit and receive units of the second split transmit and receive media access controller.

19. (Currently amended) An integrated circuit comprising:

at least a portion of a first split transmit and receive media access controller;

the split transmit and receive media access controller having a transmit unit and a receive unit physically separated from one another;

wherein the integrated circuit comprises an interface for directing signals between the transmit unit and the receive unit of the first split transmit and receive media access controller, the interface being configured to multiplex the signals with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive media access controller;

wherein the first and second split transmit and receive media access controllers have respective distinct addresses encoded by particular values of information bits sent over the interface and said information bits are decoded in order to distinguish a first signal sent between the transmit and receive units of the first split transmit and receive media access controller from a second signal sent between the transmit and receive units of the second split transmit and receive media access controller.

20. (Original) The integrated circuit of claim 19 wherein one or more of the transmit units are implemented in a first region of the integrated circuit, and one or more of the receive units are implemented in a second region of the integrated circuit, remote from the first region.

21. (Original) The integrated circuit of claim 19 wherein one or more of the transmit units are implemented on the integrated circuit and one or more of the receive units are implemented on another integrated circuit.

22. (Original) The integrated circuit of claim 19 wherein one or more of the receive units are implemented on the integrated circuit and one or more of the transmit units are implemented on another integrated circuit.